AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A method of manufacturing a Metal Oxide Semiconductor (MOS) transistor, comprising:

forming an active area in a substrate, wherein said active area is bounded by an isolation structure; and

placing at least one stress adjustor adjacent said active area, wherein said stress adjustor is positioned to modify a mobility of a majority carrier within a channel region of said MOS transistor, wherein placing said stress adjustor includes removing portions of said silicon substrate to form at least two trenches, wherein a portion of said silicon substrate remaining between said at least two trenches forms said stress adjustor and filling said trenches with a material comprising said isolation structure, wherein said stress adjustor and a first of said at least two trenches are located between a portion of a second of said at least two trenches and said active area,

wherein a long dimension of the at least one stress adjustor is placed parallel to a flow of current through said MOS transistors and is substantially equal to a gate length of said MOS transistor, the stress adjustor being positioned proximate a channel region of the MOS transistor.

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (original) The method as recited in Claim 1, wherein said stress adjustor is configured to decrease a compressive stress imparted from said isolation structure to said channel region.

7. (original) The method as recited in Claim 1, wherein said stress adjustor is configured to increase a compressive stress imparted from said isolation structure to said channel region.

Claims 8-20 (cancelled)

21. (previously presented) The method of claim 1, wherein the step of placing the at least one stress adjuster adjacent the active area comprises placing the at least one stress adjuster between about 50 nanometers and about 300 nanometers from said active area.

22. (currently amended) The method of claim 1, wherein a long dimension of ~~the~~ at least one additional stress adjustor is placed perpendicular to a flow of current through said MOS transistors and is substantially equal to a gate width of said MOS transistor.

23. (cancelled).

24. (New) A method of manufacturing a Metal Oxide Semiconductor (MOS) transistor, comprising:

forming an active area in a substrate, wherein said active area is bounded by an isolation structure; and

placing at least one stress adjustor adjacent said active area, wherein said stress adjustor is positioned to modify a mobility of a majority carrier within a channel region of said MOS transistor, wherein placing said stress adjustor includes removing portions of said silicon substrate to form at least two trenches, wherein a portion of said silicon substrate remaining between said at least two trenches forms said stress adjustor and filling said trenches with a material comprising said isolation structure, wherein said stress adjustor and a first of said at least two trenches are located between a portion of a second of said at least two trenches and said active area, the first trench having a width defining a distance between the stress adjustor and the active area, with the proviso that each stress adjustor formed adjacent the active area is positioned a substantially constant distance from the active area for approximately the entire length of the stress adjustor.

25. (New) The method as recited in Claim 1, wherein said stress adjustor is configured to decrease a compressive stress imparted from said isolation structure to

said channel region.

26. (New) The method as recited in Claim 1, wherein said stress adjustor is configured to increase a compressive stress imparted from said isolation structure to said channel region.

27. (New) The method of claim 1, wherein the step of placing the at least one stress adjuster adjacent the active area comprises placing the at least one stress adjuster between about 50 nanometers and about 300 nanometers from said active area.

28. (New) The method of claim 1, wherein a long dimension of the at least one stress adjustor is placed perpendicular to a flow of current through said MOS transistors and is substantially equal to a gate width of said MOS transistor.

29. (New) The method of claim 1, wherein a long dimension of the at least one stress adjustor is placed parallel to a flow of current through said MOS transistors and is substantially equal to a gate length of said MOS transistor.